MODERN POWER DEVICES

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mined by planar junction breakdown (see Section 3.6.1). To obtain a reduction in the electric field and an increase in the breakdown voltage, it is essential to control the implanted charge so that the implanted region becomes completely depleted under reverse bias. This occurs when the dose of the implanted charge ranges from 60 to 80% of the charge obtained by taking the product of the dielectric constant for silicon and the maximum electric field at breakdown for the parallel-plane case. With this charge, breakdown voltages to within 95% of the parallel-plane case can be achieved.

Although this termination technique is very promising for achieving close to the ideal parallel-plane junction breakdown voltage, two problems have been encountered. First, the presence of surface charge over the implanted region can strongly alter the electric field distribution. The optimum ion-implant doses are in the range of 10^{11} to 10^{12} charges/cm^2, which are comparable to surface charges arising from typical passivation processes. This can cause high electric fields to arise at either points A or B and wide variations in breakdown voltage from device to device across a wafer. Second, the high electric fields near the surface at points A and B can cause excessive leakage current flow. When applied with adequate control over the implant dose, however, the junction termination extension approach offers the possibility for achieving nearly ideal parallel-plane junction breakdown voltage by using a process that is compatible with modern device processing [28].

3.6.7. Field Plates

In previous sections it was shown that the electric field at the surface of a planar diffused junction is higher than in the parallel-plane junction because of depletion layer curvature effects. The depletion layer curvature can be controlled by altering the surface potential. The simplest method for achieving this is by placing a metal field plate at the edge of the planar junction as illustrated in Fig. 3.44. By altering the potential on the field plate, the depletion layer shape can be adjusted. When a positive bias is applied to the metal field plate with respect to the N-type substrate, it will attract electrons to the surface and cause the depletion layer to shrink as illustrated by case A. If a negative bias is applied to the field plate, it will drive away electrons from the surface, causing the depletion layer to expand as illustrated in case C. The latter phenomenon can be expected to increase the breakdown voltage. This has been observed experimentally [18]. It has been found that the breakdown voltage of the diode with field plate is related to the field plate potential V_{FP} by

$$V_D = mV_{FP} + \text{constant} \tag{3.63}$$

where $m \simeq 1$. The value for m is closer to unity for small oxide thicknesses. With sufficient bias on the field plate, the breakdown voltage of the planar diode can be made to approach the parallel-plane value.

In devices it is impractical to provide a separate bias to control the potential on the field plate. Instead, the field plate is created by merely extending the

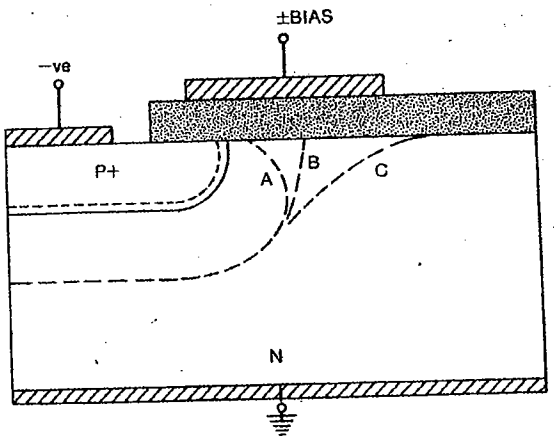

Fig. 3.44. Planar junction with field plate at edge.

junction metallization over the oxide as shown in Fig. 3.45. The presence of the field plate at the diffusion region potential forces the depletion layer to extend at the surface beyond the edge of the field plate. This reduces the depletion layer curvature and reduces the electric field at point *A*. However, a high electric field can occur at the edge of the field plate at point *B*.

Numerical analysis of the potential distribution for a planar junction with a field plate tied to its highly doped side has been performed for a variety of substrate doping concentrations and oxide thicknesses [19]. The analysis shows a high electric field arising at the edge of the field plate if the oxide thickness is small. The calculated value of the maximum ionization integral near the edge of the field plate is shown in Fig. 3.46. In this figure the ionization integral has been normalized to the value in the parallel-plane portion of the junction. The

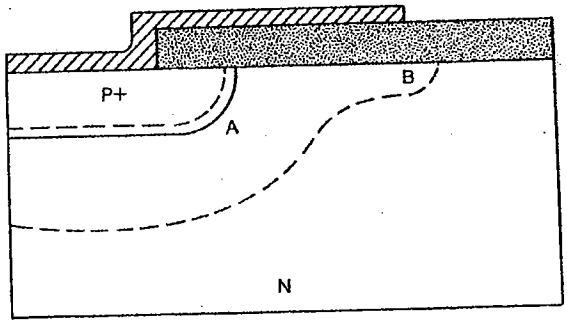

Fig. 3.45. Planar junction with field plate formed by extending the metallization over an oxide at the junction edge.

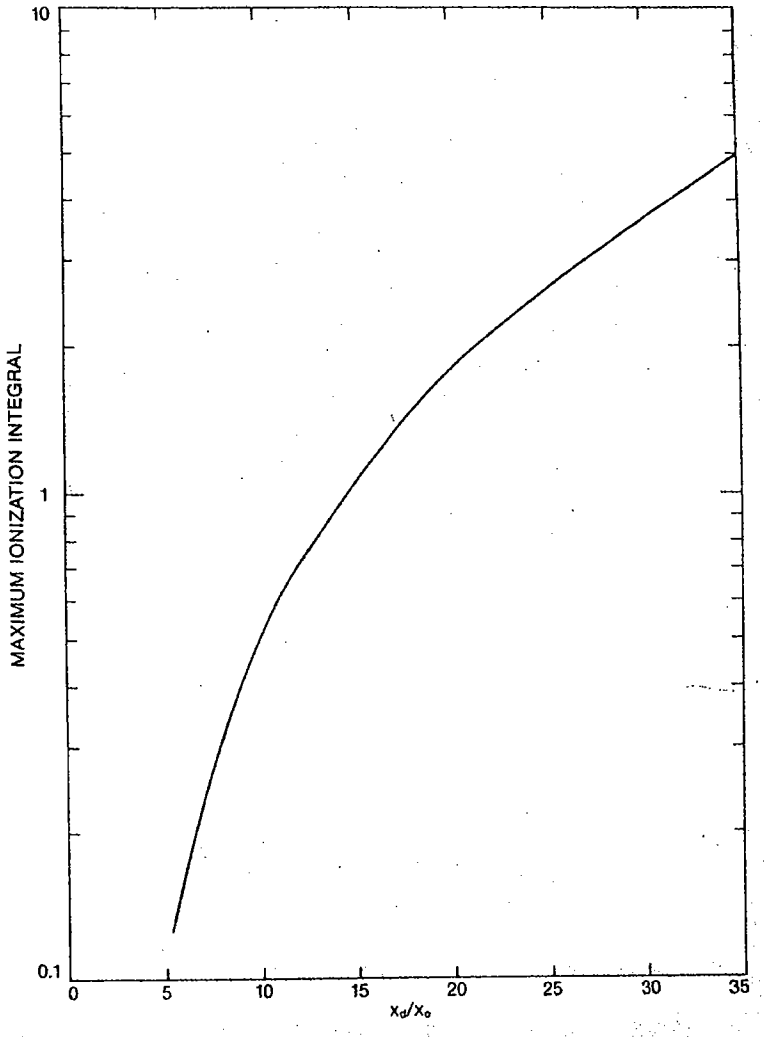

Fig. 3.46. Maximum ionization integral at the edge of a planar junction with field plate. (After Ref. 19, reprinted with permission from *Solid State Electronics*.)

term X_d is the depletion layer width, and X_o is the oxide thickness. To avoid breakdown at the edge of the field plate, it is necessary to use an oxide thickness sufficiently large to obtain X_d/X_o less than 12. However, the results in Fig. 3.46 were obtained without including the effect of curvature at the metallurgical junction. As the oxide thickness increases, the influence of the field plate on the junction curvature becomes smaller, and breakdown can now occur at the

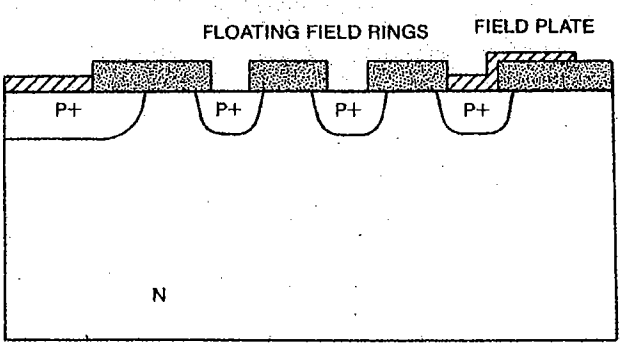

Fig. 3.47. Device termination combining floating field rings with a field plate.

metallurgical junction as a result of a high electric field at point *A* as in the case of a planar junction without the field plate. An optimum oxide thickness is, therefore, dictated to balance the peak electric fields that occur at points *A* and *B*.

An alternative to this compromise is to tailor the oxide thickness from small values near the junction to thicker values near the edge of the field plate. This requires a complex device fabrication process that is often unwarranted by the gain in breakdown voltage. A more common practice is to use the field plate in conjunction with floating field rings to achieve high breakdown voltage as illustrated in Fig. 3.47. The field plate is tied to the last floating field plate and extends beyond its edge. Field plates must not be placed between the main junction and the floating field rings or between adjacent floating field rings because they will transfer the potential between these regions and destroy the ability of the floating field rings to enhance the breakdown voltage.

3.7. OPEN-BASE TRANSISTOR BREAKDOWN

The breakdown voltage of *P–N* junctions with various junction terminations was considered in the previous sections. In these cases, the maximum achievable breakdown voltage is that of a parallel-plane *P–N* junction. However, many power devices contain back-to-back *P–N* junctions with floating middle regions. The maximum voltage blocking capability of these devices is limited by the open-base transistor breakdown of the parasitic transistor formed in these structures [20]. The influence on the breakdown voltage of the resistivity and the spacing between the *P–N* junctions in these devices is discussed in the paragraphs that follow in this section.

The open-base transistor structure is shown in the inset of Fig. 3.48 with one of the *P–N* junctions reverse-biased. This region of the device then acts as the collector and the other junction, as the emitter. When the width of the